REMARKS

In response to the Office Action mailed January 13, 2006 Applicants respectfully request reconsideration. Applicants appreciate the Examiner's detailed response, at pages 20-23 of the Office Action, to the arguments made in Applicants' response of October 13, 2005. Claims 1-18 were previously pending in this application and claims 1, 10, and 16 are amended herein. The application as presented is believed to be in condition for allowance.

Rejections Under 35 U.S.C. §112

The Office Action rejects claims 16-18 under 35 U.S.C. §112, second paragraph, asserting that these claims are indefinite because there is insufficient antecedent basis for the phrase "the execution unit" in claim 16. Applicant has amended the claim to address this issue. Accordingly, it is respectfully requested that this rejection be withdrawn.

Rejections Under 35 U.S.C. §103

The Office Action rejects claims 1-5, 8-10, 12, 14, and 16 under 35 U.S.C. §103(a) as purportedly being obvious over Song (5,546,599) in view of Grochowski (6,353,883). The Office Action further rejects claims 6, 7, 11, 13, 15, 17, and 18 under 35 U.S.C. §103(a) as purportedly being obvious over Song and Grochowski in combination with various other references. Each of these rejections is respectfully traversed and the arguments made in Applicants' response of October 13, 2005 are incorporated herein by reference.

Summary of Embodiments of the Invention

To assist the Examiner in appreciating certain aspects of the invention, Applicants provide a summary of an example of embodiments of the invention disclosed in the specification. The specification discloses that, on detection of a breakpoint, an emulation unit may take over control of the processor for debugging purposes. However, in a predicated processor, if the breakpoint is caused by an instruction whose guard value eventually resolves as false (i.e., an instruction that would never have executed), then the emulation unit taking over

control of the processor as a result of that instruction may cause unnecessary intrusion into the processor's execution. *See* Applicants' specification, page 1, line 20 – page 2, line 8.

This problem is addressed by providing an emulation unit that operates in either a precise watch mode or non-precise watch mode. In the precise watch mode, upon detection of a breakpoint instruction, subsequent instructions are not permitted to enter the execution pipeline past the decode/dispatch stage until the guard value of the breakpoint instruction is resolved. That is, the emulation unit causes the decode unit to issue a request for guard resolution. If the guard value is false, then the emulation unit may allow the execution pipeline to continue to normally. If the guard value is true, then the emulation unit may take over operation of the processor for debug purposes. This approach is advantageous because the state of the registers and memory of the processor when the emulator takes over control is the same as the state just before the breakpoint. However, the performance of the processor has been degraded, while waiting for the guard value of the breakpoint instruction to be resolved. *See* Applicants' specification, page 3, lines 22-30 and page 10, lines 8-21.

In the non-precise watch mode, when the emulation unit detects a breakpoint instruction, subsequent instructions are allowed to continue through the execution pipeline normally. Eventually, the guard value of the breakpoint instruction will be resolved. If the guard value is resolved as true, then the emulation unit may take over operation of the processor for debugging purposes. However, by the time the guard value is resolved, other instructions may have entered the pipeline. This is disadvantageous because the state of the processor at the time of debugging may be slightly different than its state at the time the breakpoint instruction was detected, making debugging slightly more complex. Nevertheless, this approach avoids halting the pipeline on detection of a breakpoint instruction to wait for guard values to be resolved, as in the precise watch mode. *See* Applicants' specification, page 10, line 22 – page 11, line 10.

The foregoing summary is provided merely to assist the Examiner in appreciating various aspects of the present invention. The summary may not apply to each of the independent claims, and the language of the independent claims may differ in material respects from the summary provided. The Examiner is requested to give a careful consideration to the language of each of the independent claims and to address each on its own merits, without relying on the summary

provided above. Applicants do not rely on the summary to distinguish any of the claims of the present invention over the prior art, but rather, rely only upon the arguments provided below.

Claim 1

Applicants maintain that neither Song nor Grochowski, whether taken alone or in combination, discloses or suggests the concept of a decode unit in a predicated pipelined processor that has two modes, wherein in a first mode (i.e., a precise watch mode) an instruction that causes a breakpoint is prevented from executing until its guard value is resolved and in a second mode (i.e., a non-precise watch mode) an instruction that causes a breakpoint is allowed to execute before its guard value is resolved.

Claim 1, as amended, recites, "[a] computer system for executing predicated instructions wherein each instruction includes a guard, the value of which determines whether or not that instruction is executed, the computer system comprising: a fetch unit for fetching instructions to be executed; a decode unit for decoding said instructions; at least one pipelined execution unit for executing decoded instructions and being associated with a guard register file holding values of the guards to allow resolution of the guards to be made; and an emulation unit including control circuitry which cooperates with the decode unit to selectively control the decode unit to implement a precise watch mode or a non-precise watch mode on detection of a breakpoint caused by a fetched instruction having a specified program count or a fetched instruction having a specified opcode, wherein when the decode unit implements the precise watch mode, the fetched instruction causing the breakpoint and at least one subsequent instruction are not permitted to be executed until after a guard value associated with the fetched instruction is resolved and, when the decode unit implements the non-precise watch mode, the instruction causing the breakpoint and at least one subsequent instruction are permitted to be executed before the guard value associated with the fetched instruction is resolved.

The Office Action states that, "applicant has not tied together the guard concept and the watch-mode concepts. Based on the claim language, applicant just has a mode where guard resolution is awaited and this would happen in any guarded/predicated system." *See* Office Action, page 6, lines 5-7. Applicants disagree that these concepts are not tied together in claim

1, as previously pending. Nevertheless, Applicants have amended claim 1 to make even more explicit the notion that when the debug unit is in the precise watch mode, an instruction causing a breakpoint and a subsequent instruction are not permitted to be executed until **after the guard value associated with the instruction is resolved**, and when the debug unit is in the non-precise watch mode, an instruction causing a breakpoint and subsequent instruction are permitted to be executed **before the guard value associated with the instruction is resolved**.

Neither Song nor Grochowski discloses or suggests a decode unit that is selectively controlled to implement either the precise watch mode and the non-precise watch mode. Song discloses that an instruction that causes an exception may not be executed until the exception is resolved (Song, col. 10, lines 22-37). Song also discloses that when the processor is in an imprecise nonrecoverable floating point exception mode and a floating point exception condition occurs, the processor, when it handles the exception, is permitted to be in a state where it has completed a variable number of instructions beyond the floating point instruction that caused the exception (Song, col. 22, lines 16-29).

The Office Action concedes that Song does not teach the use of predicated instructions, wherein each instruction is associated with a guard value, which indicates whether or not the instruction is executed. Thus, Song does not disclose or suggest, that in a precise watch mode, "the fetched instruction causing the breakpoint and subsequent instructions are not permitted to be executed until a guard value associated with the fetched instruction is resolved" and in a non-precise watch mode, "the instruction causing the breakpoint and subsequent instructions are permitted to be executed before the guard value is resolved." In Song, whether an instruction causing an exception is executed before the exception is handled depends solely on the mode of the processor, but does not depend on resolution of a guard value associated with the instruction.

Grochowski does not cure this infirmity of Song. While Grochowski discloses the use of predicated instructions, **Grochowski does not disclose or suggest that the determination of whether to execute an instruction before resolution of its guard value is based on whether the decode unit is in a precise watch mode or a non-precise watch mode.** Rather, Grochowski discloses that the determination of whether to execute an instruction before resolution of its guard value is based on the probability that the guard value will indicate that the

instruction is to be executed. Specifically, at column 3, lines 25-35, Grochowski states, "[g]iven these conditions, the IF-THEN and ADD instructions following the COMPARE instruction can be executed before the COMPARE instruction completes if the value of predicate p2 can be predicted. Unfortunately, if p2 is incorrectly predicted, the recovery time may take, for example, ten or more clocks. Therefore, it is important that p2 be predicted only if there is a high likelihood that the prediction will be correct. Otherwise, it is best to wait the three clocks until the COMPARE instruction completes and the actual predicated value for p2 is determined before executing the IF-THEN and ADD instructions."

Thus, neither Song nor Grochowski discloses or suggests that the determination of whether to execute an instruction before resolution of its guard value is based on whether the decode unit is in a precise watch mode or a non-precise watch mode.

In addition, claim 1 requires, "an emulation unit including control circuitry which cooperates with the decode unit to selectively control the decode unit to implement a precise watch mode or a non-precise watch mode." That is, claim 1 requires that the emulation unit selectively control whether the debug unit is in the precise watch mode or the non-precise watch mode. Neither Song nor Grochowski discloses this limitation of claim 1. As discussed above, in Grochowski, the decision whether to execute an instruction before determination of the predicated value depends on the probability that predicted predicate value will be correct. While Song does not explicitly disclose how the imprecise non-recoverable floating point exception mode is selected, it appears that this mode is selected by the user. In any case, Song does not disclose that the mode is selected under the control of an emulation unit.

The Office Action states, "the examiner asserts that the prior art has taught emulation circuitry since it essentially operates in the same manner as applicants' circuitry. To debug is to find and remove errors or bugs in a program. The circuitry of Song does just this as it detects exceptions (errors) and corrects them." *See* Office Action ¶34 at page 22. Applicants do not deny that Song discloses handling exceptions. However, in Song, the handling of exceptions is unrelated to whether or not the processor is in the imprecise non-recoverable floating point exception mode. Song does not disclose an emulation unit that selectively controls whether the decode unit implements a precise watch mode or a non-precise watch mode.

Thus, for at least the reasons discussed above, claim 1 patentably distinguishes over Song and Grochowski, whether taken alone or in combination. Accordingly it is respectfully requested that the rejection of claim 1 under 35 U.S.C. §103(a) be withdrawn.

Claims 2-9 depend from claim 1 and are patentable for at least the same reasons. Accordingly, it is respectfully requested that the rejection of claims 2-9 be withdrawn.

Claim 10

Claim 10, as amended, is directed to a method of debugging an on-chip processor which is arranged to execute predicated instructions wherein each instruction includes a guard, the value of which determines whether or not that instruction is executed. The method comprises: fetching instructions to be executed; decoding said instructions; executing decoded instructions, said executing step including resolving values of the guards of the instructions; and detecting instructions which have a debug effect based on a program count or an opcode of the instructions and acting on said instructions in dependence on whether the processor is in a precise watch mode or a non-precise watch mode wherein, according to the precise watch mode, an instruction having a debug effect and at least one subsequent instruction are not permitted to be executed until after a guard value associated with the instruction is resolved and, according to a non-precise watch mode, the instruction and the at least one subsequent instruction are permitted to be executed before the guard value is resolved.

As should be clear from the discussion above in, neither Song nor Grochowski teaches or suggests, "detecting instructions which have a debug effect based on a program count or an opcode of the instructions and acting on said instructions in dependence on whether the processor is in a precise watch mode or a non-precise watch mode wherein, according to the precise watch mode, an instruction having a debug effect and at least one subsequent instruction are not permitted to be executed until after a guard value associated with the instruction is resolved and, according to a non-precise watch mode, the instruction and the at least one subsequent instruction are permitted to be executed before the guard value is resolved," as recited in claim 10.

Thus, claim 10 patentably distinguishes over Song and Grochowski, whether taken alone or in combination. Accordingly, it is respectfully requested that rejection of claim 10 under 35 U.S.C. §103(a) be withdrawn.

Claims 11-15 depend from claim 10 and are patentable for at least the same reasons. Accordingly, it is respectfully requested that the rejection of claims 11-15 be withdrawn.

Claim 16

Claim 16, as amended, is directed to a computer system for executing predicated instructions wherein each instruction includes a guard, the value of which determines whether or not that instruction is executed. The computer system comprises: a fetch unit for fetching instructions to be executed; a decode unit for decoding said instructions; at least one pipelined execution unit for executing decoded instructions and being associated with a guard register file holding values of the guards to allow resolution of the guards to be made; and an emulation unit including control circuitry which cooperates with the decode unit to selectively control the decode unit to implement a precise watch mode or a non-precise watch mode on detection of a breakpoint caused by a fetched instruction having a specified program count or a fetched instruction having a specified opcode, wherein when the decode unit implements the precise watch mode, the fetched instruction causing the breakpoint and at least one subsequent instruction are not permitted to be executed until after a guard value associated with the fetched instruction is resolved and, when the decode unit implements the non-precise watch mode, the fetched instruction causing the breakpoint and at least one subsequent instruction are permitted to be executed before the guard value is resolved, wherein, when the decode unit implements the precise watch mode, the emulation unit is operable to issue a request to the execution pipeline for guard resolution, the guard resolution being transmitted to the control circuitry of the emulation unit which is responsive thereto to control operation of the decode unit.

As should be clear from the discussion above, neither Song nor Grochowski, discloses or suggests, "an emulation unit including control circuitry which cooperates with the decode unit to selectively control the decode unit to implement a precise watch mode or a non-precise watch mode on detection of a breakpoint caused by a fetched instruction having a specified program count or a fetched instruction having a specified opcode, wherein when the decode unit

implements the precise watch mode, the fetched instruction causing the breakpoint and at least one subsequent instruction are not permitted to be executed until after a guard value associated with the fetched instruction is resolved and, when the decode unit implements the non-precise watch mode, the fetched instruction causing the breakpoint and at least one subsequent instruction are permitted to be executed before the guard value is resolved, wherein, when the decode unit implements the precise watch mode, the emulation unit is operable to issue a request to the execution pipeline for guard resolution, the guard resolution being transmitted to the control circuitry of the emulation unit which is responsive thereto to control operation of the decode unit," as recited in claim 16.

Thus, claim 16 patentably distinguishes over Song and Grochowski, whether taken alone or in combination. Accordingly, it is respectfully requested that rejection of claim 16 under 35 U.S.C. §103(a) be withdrawn.

Claims 17 and 18 depend from claim 16 and are patentable for at least the same reasons. Accordingly, it is respectfully requested that the rejection of claims 17 and 18 be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

Andrew Cofler et al.

By: _____

James H. Morris, Reg. No. 46,066
WOLF, GREENFIELD & SACKS, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210
Tel. (617) 720-3500

Attorney's Docket No.: S1022.80583US00
Dated: April 13, 2006